P-Channel Enhancement Mode Field Effect Transistor

Top View

S ☐	1 ○	8 ☐ D
S ☐	2	7 ☐ D
S ☐	3	6 ☐ D
G ☐	4	5 ☐ D

SOP-8

Product Summary

- V_{DS} -30V
- I_D -12A
- $R_{DS(ON)}$(at V_{GS}=-20V)   ＜11mohm
- $R_{DS(ON)}$(at V_{GS}=-10V)   ＜13mohm
- $R_{DS(ON)}$(at V_{GS}=-6V)   ＜17mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V)   ＜27mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Power management
- Load switch

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-30	V
Gate-source Voltage	V_{GS}	±20	V
Drain Current	I_D	-12	A
Pulsed Drain Current [A]	I_{DM}	-55	A
Single Pulse Avalanche Energy [B]	E_{AS}	105	mJ
Total Power Dissipation @ T_A=25℃ [C]	P_D	3.2	W
Thermal Resistance Junction-to-Ambient @ Steady State [D]	$R_{θJA}$	39	℃ / W
Junction and Storage Temperature Range	T_J ,T_{STG}	-55～+150	℃

■ Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV$_{DSS}$	V$_{GS}$= 0V, I$_D$=-250μA	-30			V
Zero Gate Voltage Drain Current	I$_{DSS}$	V$_{DS}$=-30V,V$_{GS}$=0V,T$_C$=25℃			-1	μA
Gate-Body Leakage Current	I$_{GSS}$	V$_{GS}$= ±20V, V$_{DS}$=0V			±100	nA
Gate Threshold Voltage	V$_{GS(th)}$	V$_{DS}$= V$_{GS}$, I$_D$=-250μA	-1.2	-1.7	-2.8	V
Static Drain-Source On-Resistance	R$_{DS(ON)}$	V$_{GS}$= -20V, I$_D$=-12A		9.0	11	mΩ
		V$_{GS}$= -10V, I$_D$=-10A		10.2	13	
		V$_{GS}$= -6.0V, I$_D$=-8A		12.3	17	
		V$_{GS}$= -4.5V, I$_D$=-8A		16	27	
Diode Forward Voltage	V$_{SD}$	I$_S$=-12A,V$_{GS}$=0V		-0.8	-1.2	V
Dynamic Parameters						
Input Capacitance	C$_{iss}$	V$_{DS}$=-15V,V$_{GS}$=0V,f=1MHZ		2152		pF
Output Capacitance	C$_{oss}$			308		
Reverse Transfer Capacitance	C$_{rss}$			242		
Switching Parameters						
Total Gate Charge	Q$_g$	V$_{GS}$= -10V,V$_{DS}$= -15V,I$_D$= -12A		40.1		nC
Gate Source Charge	Q$_{gs}$			8.4		
Gate Drain Charge	Q$_{gd}$			8.6		
Reverse Recovery Charge	Q$_{rr}$	I$_F$= -12A, di/dt= 100A/us		7.8		nC
Reverse Recovery Time	t$_{rr}$			18		
Turn-on Delay Time	t$_{D(on)}$	V$_{GS}$= -10V,V$_{DD}$= -15V, I$_D$= -1A, R$_{GEN}$= 2.5Ω		8		ns
Turn-on Rise Time	t$_r$			19		
Turn-off Delay Time	t$_{D(off)}$			75		
Turn-off Fall Time	t$_f$			46		

A.   Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B.   R$_{θJA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R$_{θJL}$ is guaranteed by design, while R$_{θJA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

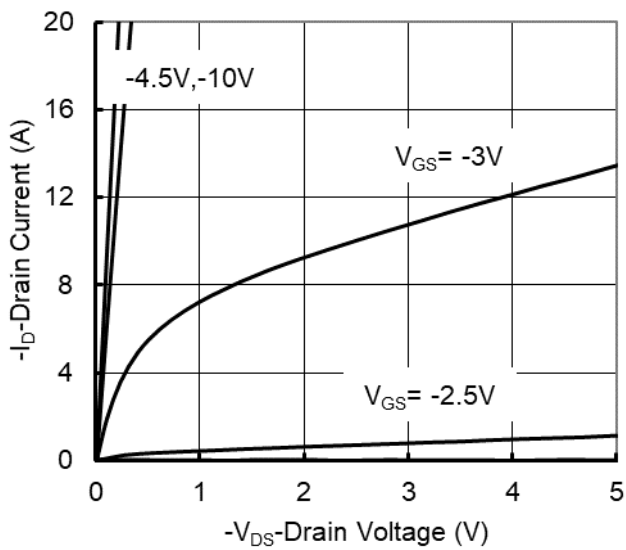■ **Typical Performance Characteristics**

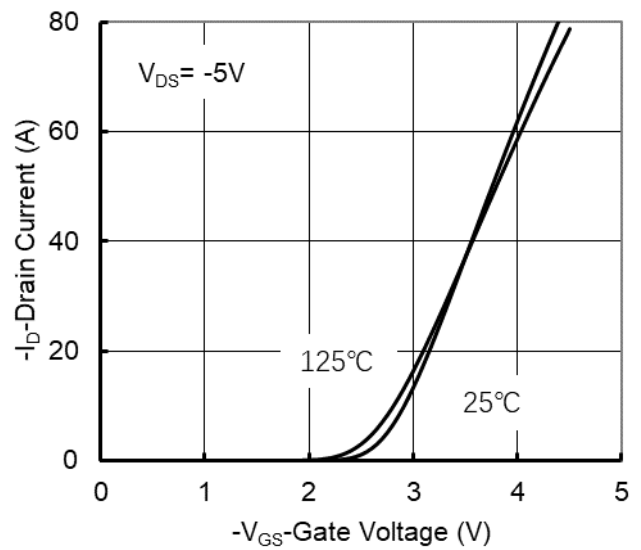Figure 1. Output Characteristics
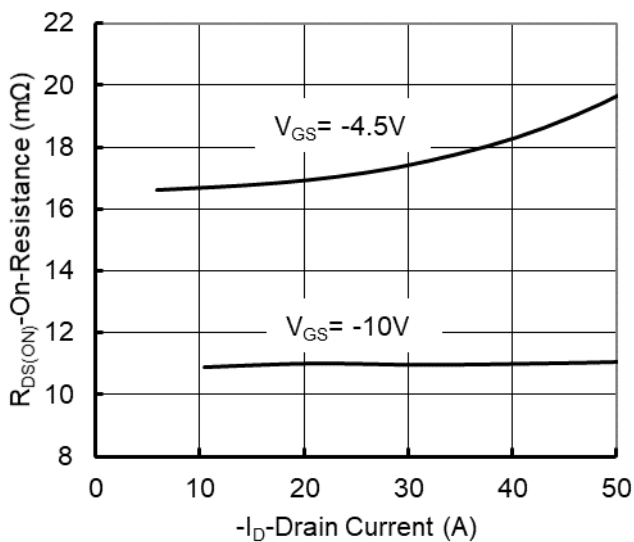

Figure 2. Transfer Characteristics

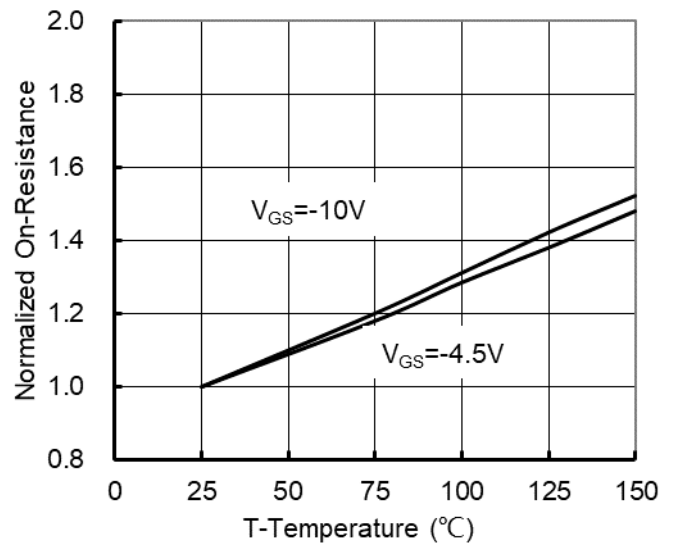Figure 3. On-Resistance vs. Drain Current
and Gate Voltage

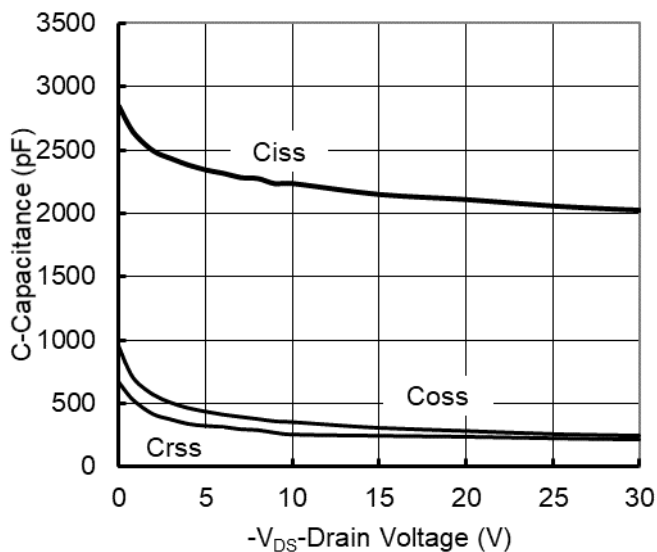Figure 4. On-Resistance vs. Junction Temperature
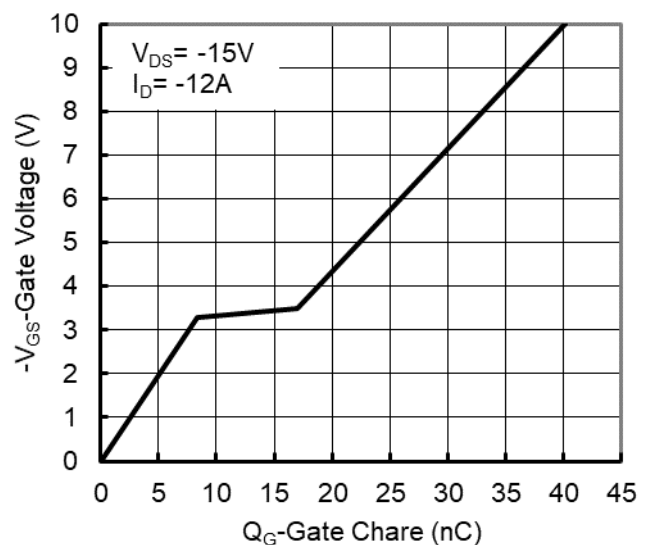

Figure 5. Capacitance Characteristics
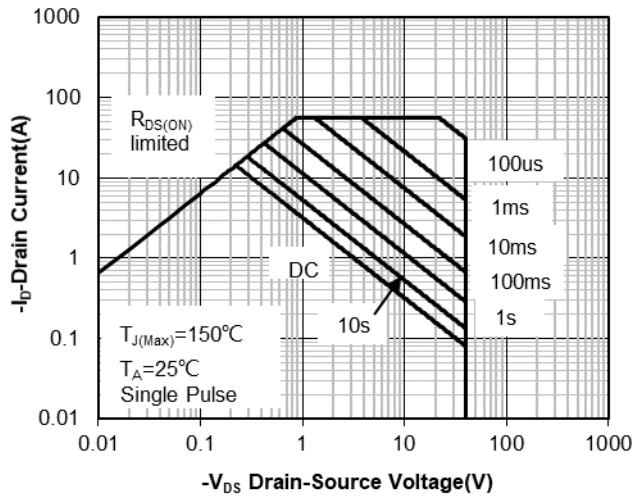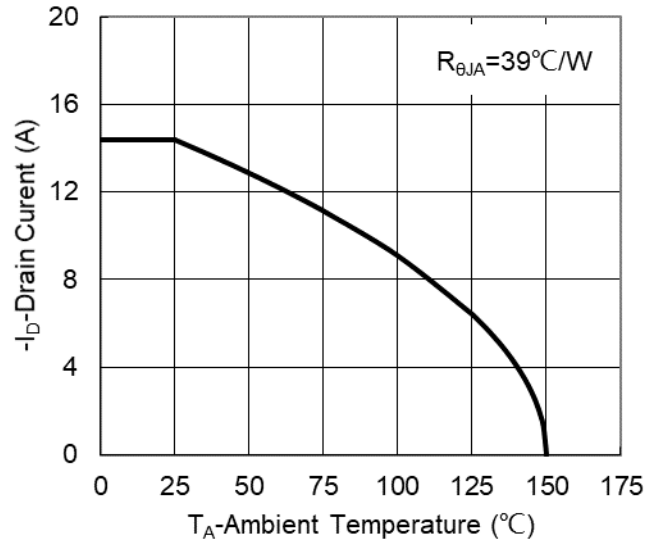

Figure 6. Gate Charge

Figure 7. Safe Operation Area

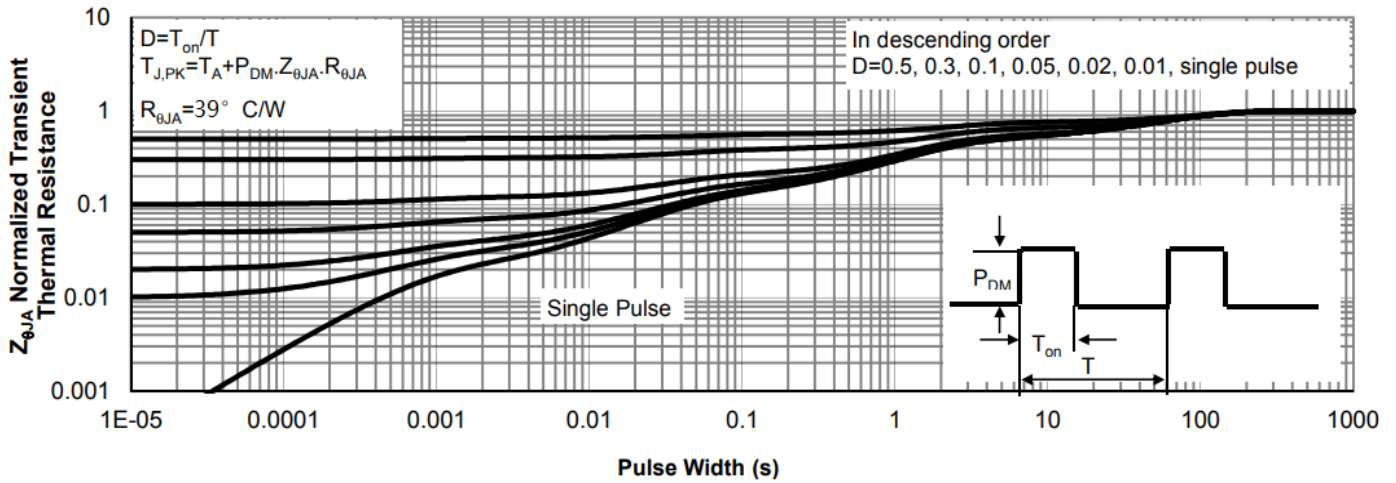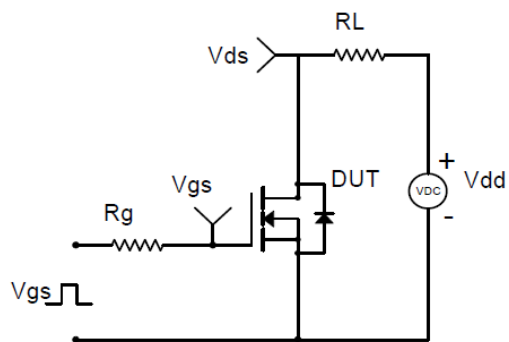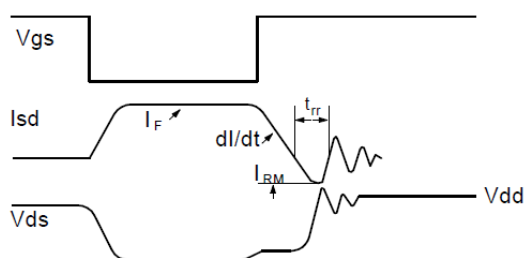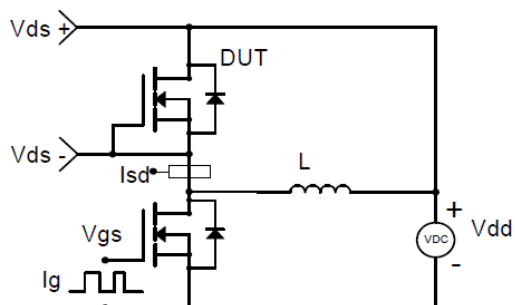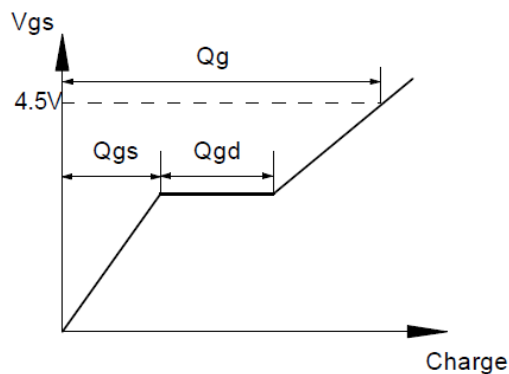Figure 8. Maximum Continuous Drain Current
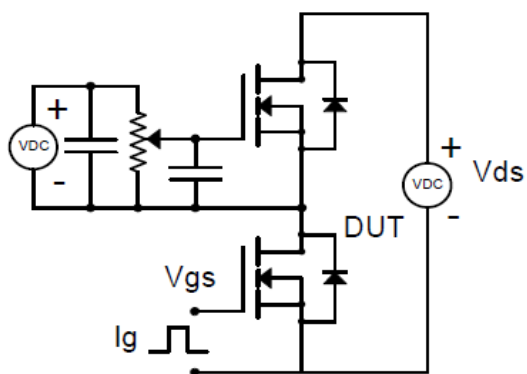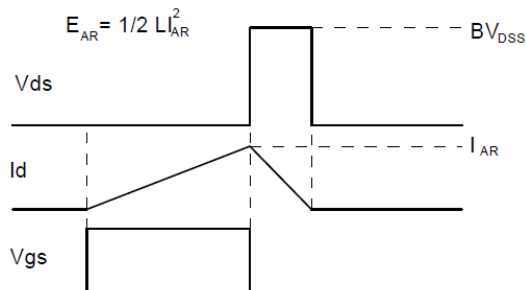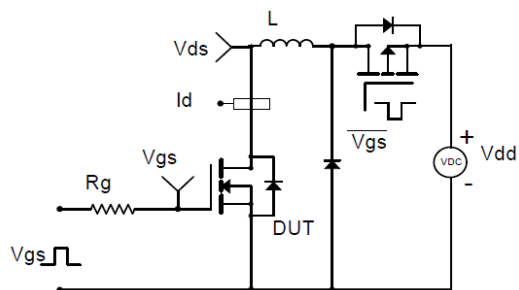vs Ambient Temperature

Figure 9. Normalized Maximum Transient Thermal Impedance

Resistive Switching Test Circuit & Waveforms
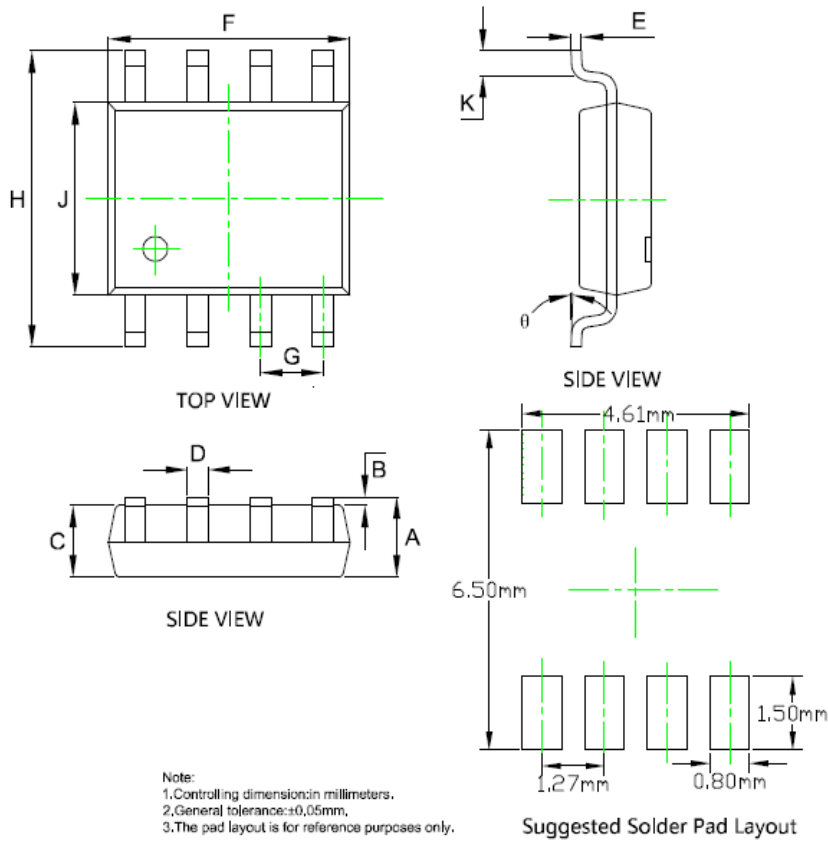

Diode Recovery Test Circuit & Waveforms

Gate Charge Test Circuit & Waveform

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■ SOP-8 Package information

TOP VIEW

SIDE VIEW

SIDE VIEW

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

Suggested Solder Pad Layout

SYMBOL	INCHES		MIllimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

DIMENSIONS